What is claimed is:

1. A method of manufacturing a semiconductor device comprising:

forming a resin layer on a semiconductor substrate in which a plurality of integrated circuits are formed;

forming a plurality of recesses in a surface of the resin layer;

forming an interconnecting line on the resin layer, to pass along any one of the recesses; and

cutting the semiconductor substrate into a plurality of semiconductor chips;

wherein each of the recesses is formed to have an opening width less than a thickness of the interconnecting line, and to have a depth of at least 1 μ m.

2. The method of manufacturing a semiconductor device as defined in claim 1,

wherein the resin layer is formed of a photosensitive resin precursor,

wherein in the step of forming the recesses, photolithography using a mask is applied, and

wherein the mask includes a transparent-and-opaque pattern for carrying out light irradiation with too fine pattern for the photosensitive resin precursor to be resolved.

3. The method of manufacturing a semiconductor device as defined in claim 2,

wherein the photosensitive resin precursor is a negative type including an insoluble light-sensitive portion, and

wherein the transparent-and-opaque pattern includes an opaque portion having a width less than or equal to the thickness of the interconnecting line.

4. The method of manufacturing a semiconductor device as defined in claim 3,

wherein the width of the opaque portion is less than or equal to one-fourths of a

thickness of the resin layer.

5. The method of manufacturing a semiconductor device as defined in claim 1, further comprising:

roughening the surface of the resin layer including inner surfaces of the recesses, after forming the recesses and before forming the interconnecting line.

6. The method of manufacturing a semiconductor device as defined in claim 5, further comprising:

forming a second resin layer on the resin layer to cover at least a part of the interconnecting line, after forming the interconnecting line and before cutting the semiconductor substrate.

7. The method of manufacturing a semiconductor device as defined in claim 6, further comprising:

forming recesses and projections on a surface of the second resin layer.

8. The method of manufacturing a semiconductor device as defined in claim 7, further comprising:

forming a third resin layer on the second resin layer.

9. The method of manufacturing a semiconductor device as defined in claim 8, further comprising:

forming recesses and projections on a surface of the third resin layer.

10. A semiconductor wafer comprising:

a semiconductor substrate in which a plurality of integrated circuits are formed;

a resin layer formed on the semiconductor substrate, and having a plurality of recesses formed in a surface of the resin layer; and

an interconnecting line formed on the resin layer, to pass along any one of the recesses,

wherein each of the recesses is formed to have an opening width less than a thickness of the interconnecting line, and to have a depth of at least 1 μ m.

11. The semiconductor wafer as defined in claim 10,

wherein the opening width of each of the recesses is less than or equal to one-fourths of a thickness of the resin layer.

12. The semiconductor wafer as defined in claim 10,

wherein the recesses are formed over an entire area of the surface of the resin layer.

13. The semiconductor wafer as defined in claim 10,

wherein the interconnecting line has a land for providing an external terminal; and

wherein the recesses are formed at least in a region under the land of the resin layer.

14. The semiconductor wafer as defined in claim 10,

wherein the surface of the resin layer including inner surfaces of the recesses is roughened.

15. The semiconductor wafer as defined in claim 14,

wherein the resin layer is defined as a first resin layer, and

wherein the semiconductor wafer further comprises a second resin layer formed on the first resin layer so as to cover at least a part of the interconnecting line.

16. The semiconductor wafer as defined in claim 15,

wherein recesses and projections are formed on a surface of the second resin layer.

17. The semiconductor wafer as defined in claim 16, further comprising a third resin layer formed on the second resin layer.

18. The semiconductor wafer as defined in claim 17,

wherein recesses and projections are formed on a surface of the third resin layer.

19. The semiconductor wafer as defined in claim 18,

wherein the third resin layer is formed of a material having a higher opacity than the first and second resin layers.

20. A semiconductor device comprising:

a semiconductor chip in which a plurality of integrated circuits are formed;

a resin layer formed on the semiconductor chip, and having a plurality of recesses formed in a surface of the resin layer; and

an interconnecting line formed on the resin layer, to pass along any one of the recesses,

wherein each of the recesses is formed to have an opening width less than a thickness of the interconnecting line, and to have a depth of at least 1 μ m.

21. The semiconductor device as defined in claim 20,

wherein the opening width of each of the recesses is less than or equal to one-fourths of a thickness of the resin layer.

22. The semiconductor device as defined in claim 20,

wherein the recesses are formed over an entire area of the surface of the resin layer.

23. The semiconductor device as defined in claim 20,

wherein the interconnecting line has a land for providing an external terminal; and

wherein the recesses are formed at least in a region under the land of the resin layer.

24. The semiconductor device as defined in claim 20,

wherein the surface of the resin layer including inner surfaces of the recesses is roughened.

25. The semiconductor device as defined in claim 24,

wherein the resin layer is defined as a first resin layer, and

wherein the semiconductor device further comprises a second resin layer formed on the first resin layer so as to cover at least a part of the interconnecting line.

26. The semiconductor device as defined in claim 25,

wherein recesses and projections are formed on a surface of the second resin layer.

27. The semiconductor device as defined in claim 26, further comprising a third

resin layer formed on the second resin layer.

28. The semiconductor device as defined in claim 27,

wherein recesses and projections are formed on a surface of the third resin layer.

29. The semiconductor device as defined in claim 28,

wherein the third resin layer is formed of a material having a higher opacity than the first and second resin layers.

30. A circuit board having the semiconductor device defined in claim 20, mounted thereon.

31. An electronic instrument having the semiconductor device defined in claim 20.